IN THE SPECIFICATION

Please amend Paragraph 14 of the Specification as follows:

[14] FIGURE 2 shows a schematic circuit diagram in accordance with the present invention. PMOS transistors M21, M22 and NMOS transistors M23, M24 form the latch of a sense amplifier. The ~~gate~~ gates of the equalizing PMOS ~~transistor~~ transistors M212 and M213 are ~~is~~ connected to Sense Amplifier Equalize Signal SAEQ. Bitlines BL and BLB are connected through PMOS transistors M26 and M27 to the latch. The gate of the latch-enabling transistor M25 is connected to control signal SAEN. The outputs of inverters INV1, INV2 are fed back to the gates of access transistors M26, M27 from evaluating nodes SN1, SN2 respectively.